

**REMARKS**

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendments and the following remarks.

The Applicants originally submitted Claims 1-36 in the application. The Applicants affirm that Claims 8-14 and 26-36 were withdrawn from consideration as being non-elected claims, and are hereby cancelled pending the possible filing of a divisional application. Additionally, Claims 1 and 15 have been amended to further delineate an inherent feature of the previously claimed subject matter, and Claims 37 and 38 have been added to delineate a disclosed but unclaimed feature in accordance with the principles of the present invention. Accordingly, Claims 1-7, 15-25 and 37-38 are currently pending in the application.

**I. Rejection of Claims under 35 U.S.C. §102**

The Examiner has rejected Claims 1 and 3 under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,384,447 to Mihnea, *et al.* ("Mihnea"). As the Examiner is no doubt aware, anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference; the disclosed elements must either be disclosed expressly or inherently and must be arranged as in the rejected claims.

The Examiner asserts that Mihnea discloses source/drain regions 112, 115 including a lightly doped region 133 adjacent a heavily doped region 136. According to the Examiner, Mihnea also teaches an oppositely doped well region 128 under and within the channel region 162, and a doped region 139 located between the heavily doped region 136 and oppositely doped well region 128 having a doping concentration profile less than a doping concentration profile of the heavily doped region. (Examiner's Action, page 2). The Applicants respectfully disagree.

As illustrated in FIGURE 1, a flash memory cell of Mihnea includes a source 112, gate 148 and a drain 115. The drain 115 includes an arsenic doped region 133 abutting a phosphorous doped region 136. Between the source 112 and the drain 115 is a channel region 118 that includes heavily doped boron regions 127, 128 and a lightly doped boron region 139 thereunder. The phosphorous doped region 136 is lightly doped and abuts the lightly doped boron region 139. Column 5, lines 22-60. As further illustrated in FIGURE 1 and recited in Claim 1 of Mihnea, the heavily doped arsenic region is surrounded by the phosphorous doped region.

While Mihnea discloses a flash memory cell, the reference fails to disclose a transistor as recited in Claim 1 of the present application. More particularly, Mihnea does not disclose a source/drain including a lightly doped region located adjacent a channel region and a heavily doped region located adjacent to but not surrounded by the lightly doped region within a semiconductor substrate as recited in Claim 1. As mentioned above, the heavily doped arsenic region of Mihnea is surrounded by the phosphorous doped region (*i.e.*, the lightly doped region) thereof. The resulting structure of the source/drain region of the transistor of Claim 1 of the present application, therefore, contrasts from the drain as illustrated and described with respect to the flash memory cell of Mihnea.

Thus, Mihnea does not disclose each and every element of Claim 1, and the claims dependent thereon, and, as such, is not an anticipating reference. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection in view of Mihnea with respect to Claims 1 and 3.

## II. Rejection of Claims under 35 U.S.C. §103

The Examiner has rejected Claims 6, 7, 15-21, 24 and 25 under 35 U.S.C. §103(a) as being unpatentable over Mihnea in view of U.S. Patent Publication No. 2004/0227190 to Cai, et al ("Cai"). The Examiner asserts that Mihnea teaches the source/drain region, oppositely doped well and a doped region as discussed above. Cai is then introduced by the Examiner to disclose an LDMOS and sidewall/spacers. The Examiner believes that the combination of Mihnea and Cai renders the subject matter of Claims 6, 7, 15-21, 24 and 25 obvious. (Examiner's Action, page 3). The Applicants respectfully assert that the claimed invention is not obvious in view of the foregoing references, and that the Examiner has failed to establish a *prima facie* case of obviousness of the aforementioned claims.

For the reasons as set forth above, Mihnea fails to teach or suggest a transistor or semiconductor device having a source/drain including a lightly doped region located adjacent a channel region and a heavily doped region located adjacent to but not surrounded by the lightly doped region within a semiconductor substrate as recited in Claims 1 and 15. Mihnea, therefore, fails to teach or suggest all of the elements of Claims 1 and 15, and Cai, by the Examiner's own admission, does not even address such a structure. Thus, since Mihnea fails to teach or suggest all of the elements of Claims 1 and 15, and Cai fails to cure the deficiencies thereof, the

Examiner cannot establish a *prima facie* case of obviousness of Claims 1 and 15, or the claims dependent thereon.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 6, 7, 15-21, 24 and 25 under 35 U.S.C. §103(a). In accordance therewith, the Applicants respectfully request the Examiner withdraw the rejection.

## II. Conclusion

In view of the foregoing amendments and remarks, the Applicants now see all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-7, 15-25 and 37-38.

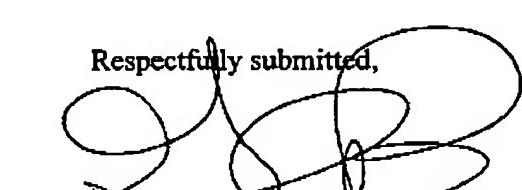
The Applicants request that the Examiner telephone the undersigned attorney of record at (972) 732-1001 if such would further expedite the prosecution of the present application. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

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June 23, 2005

Date

Respectfully submitted,



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